FAULT DIAGNOSIS FOR ANALOG ELECTRONIC CIRCUIT USING TIME RESPONSE ANALYSIS

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Abstract : - This paper addresses the fault diagnosis issue based on a simulation before test philosophy in analog electronic circuits with artificial neural networks as a tool in the development of a test strategy. The proposed system has the capability to detect and identify faulty components in an analog electronic circuit by analyzing its step response. The primary focus of the paper is to provide robust diagnosis using a simple mechanism for automatic test pattern generation while reducing test time. In this thesis a sallen key band pass filter circuit is considered for the fault diagnosis process. This proposed approach consists of obtaining the step response of fault free/faulty circuit under test. Then the settling time, delay time and the peak values from the step response are extracted for faulty and non-faulty conditions. These time response specifications are compared with the fault free circuit and processed to classify the type of fault. The artificial neural network that can provide an adaptive mechanism for the pattern classification is used for the classification of faults. By comparing the proposed work with the traditional analysis, it is proved that fault computation time is drastically reduced from the conventional analysis techniques and the proposed algorithm performs better in fault diagnosis of analog electronic circuits.

Keywords: Fault Diagnosis, Artificial neural networks, Ann Classifier, Sallen key band pass filter circuit

I. INTRODUCTION

The process of developing test strategies for electronic circuits is typically complex and costly due to the amount of manual interaction and iterations required between the test developer and currently available tools. To effectively develop test strategies, the test developer must be familiar with the test system and its instrument's capabilities. The test developer also must analyze the circuit to be tested and have some detailed knowledge of the circuit's operational characteristics. Often the test developer is also the programmer for the test system. Expert test developers rely on experience in developing test strategies. Their methodology is often an iterative, time-consuming, process. A system which automatically develops the equivalent of testing strategies directly from circuit descriptions would be a significant advance in test development. Since modeling and simulation has become a common design tool for circuit development, circuit descriptions in machine readable form are readily available.

Artificial neural networks (ANNs) have been applied in many areas such as pattern recognition, signal and image processing, etc. ANNs have the advantages of large-scale parallel processing, parallel storing, robust adaptive learning, and on-line computation. They are ideal for fault diagnosis of analog circuits with tolerances. This paper proposes an ANN based method for fault diagnosis of analog circuits with tolerances.

The difficulties encountered in analog fault diagnosis make the use of artificial neural network (ANN) quite appealing. The research presented here attempts to exploit the signature analysis capabilities of artificial neural networks to provide fault diagnosis with minimal computational cost. The proposed method is a form of SBT with ANN serving the role of the classifier. The SBT approach basically consists of obtaining the standard frequency response of the fault free/faulty circuit topology.

II. PROPOSED FAULT IDENTIFICATION ALGORITHM

1. State model of the filter circuit is derived for nominal value of the circuit components.
2. Time response of the filter circuit is simulated under different faulty conditions.
3. Time response specifications are obtained and stored in array for each faulty condition.
4. Then an ANN is trained for different faulty conditions to classify the fault.
5. The filter circuit is tested at various test frequencies and if the time response specifications lie within the corresponding predetermined limits, suitable signature is fed to

the ANN classifier which does the fault classification.

III. PREPROCESSOR

A complete fault dictionary containing all feasible conditions cannot obviously be generated because of the presence of noise.

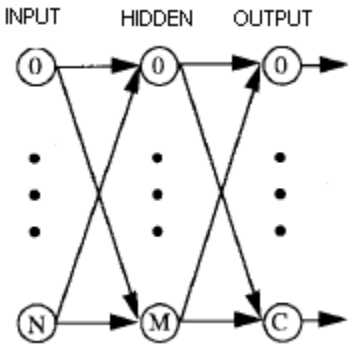

Fig. 1 Two layer BPN network

This problem is solved by giving inputs to the neural network in terms of bits—a "0" is assigned if the value observed for a specific test frequency is out of bounds; a "1" is assigned if the value observed for a specific test frequency is within bounds. That is, if $X_L \leq X_m \leq X_H$ implies ANN input = 1, else ANN input = 0.

IV. ANN CLASSIFIER

In recent years, ANNs have received great attention in many aspects of scientific research and have been applied successfully in various fields such as chemical processes, digital circuitry, control systems, etc, for ANNs provide a mechanism for adaptive pattern classification. Even in unfavorable environments, they can still have robust classification. It should be stressed that choosing a suitable ANN architecture is vital for the successful application of ANNs. To date the most popular ANN architecture is the backward propagation neural network (BPNN). One of the significant features of neural networks when applied in fault diagnosis and testing is that on-line diagnosis is fast once the network is trained. In addition, ANN classifiers require fewer fault features than traditional classifiers. Further, neural networks are capable of performing fault classification at hierarchical levels. In this paper, the back propagation network (BPN) structure provides best results for the classification task. Many other works have also had success using the BPN network. Examples include classification of sonar targets, speech recognition, and sensor interpretation. Recent successes have applied ANNs to process fault detection in chemical processes. Direct applications of ANNs for fault diagnosis can be found. Typical BPN have two or three layers of interconnecting weights.

The number of nodes in a layer and the activation function will affect the learning rate, the computational complexity, and the usefulness of the network for a specific problem wherein the best results always come from intuition and experience.

V. SALLEN KEY BAND PASS FILTER CIRCUIT

The Sallen- Key filter is a very popular active filter which can be used to create 2nd order filter stages that can be cascaded together to form larger order filters. The op-amp provides buffering between filter stages, so that each stage can be designed independently of the others. These circuits are suitable for filters which have complex conjugate poles. When implementing a particular transfer function, a designer will typically find all of the poles, and group them into real poles and complex conjugate pairs. Each of the complex conjugate pole pares are then implemented with a Sallen-Key filter, and the circuits are cascaded together to form the complete filter.

The circuit shown in Fig. 2 is the Sallen Key band pass filter circuit with the component values correspond to a nominal center frequency of 25 kHz. Each resistor has a tolerance of 5% and capacitor has a tolerance of 10%.

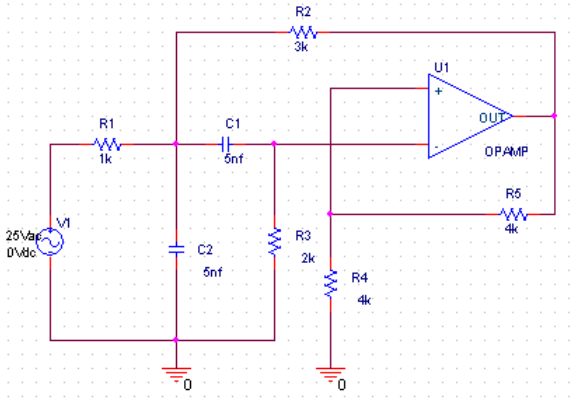

Fig. 2 Sallen key band pass filter circuit

To study the testability of the circuit, the step response is plotted for various fault conditions. The sensitivity of the output signal with respect to single faults along with the step response of the nominal circuit is given in Fig. 4 and Fig. 5. In the process, all the other components are kept at their nominal values. There are totally $2n$ single faults where n is the number of components in the circuit for which the sensitivity analysis is done.

VI. PATTERN CLASSIFIER

Since the test pattern for the filter circuit has 26 inputs (25 faults plus 1 fault-free condition), the ANN has 26 neurons in the input layer and 5 neurons in the output layer. The 5 neurons in the output layer can classify a total of 32 faults (25) and will be sufficient for classifying 25 plus 1 possible condition in our work. The number of neurons in the hidden single layer is 53. So the ANN structure boils down to 20: 53: 5. For all faults *F*1 through *F*26, the corresponding subscripts (1 through 26) indicate the fault IDs. The ANN is adaptively trained to update the weights and the bias by gradient descent method by the mean-square-error performance.

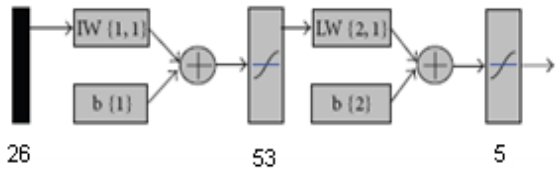

Fig. 3 Classifier for test circuit

VII. SIMULATION RESULTS

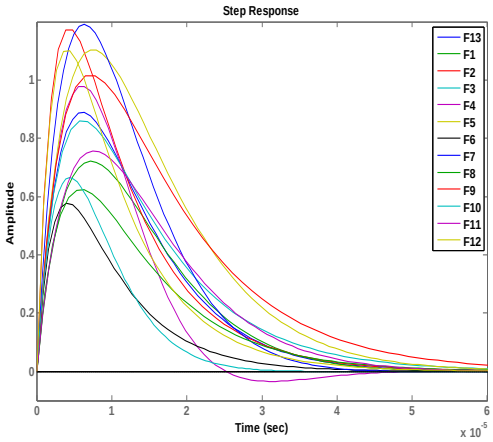

Fig. 4 Step response for single faults

Fault ID	Fault components	Settling time *10^-5 sec	Peak	Delay time *10^-6 sec
F1	R1+50	-0.0587	0.1669	-0.29
F2	R1-50	0.069	-0.2829	0.478
F3	R2+50	-0.9612	0.028	0.01
F4	R2-50	0.5017	-0.0908	-0.09
F5	R3+50	-0.8026	-0.2144	-0.33
F6	R3-50	0.674	0.311	0.476
F7	R5+50	0.6909	-0.3028	-0.08
F8	R5-50	-0.6487	0.2652	0.05
F9	C1+50	-1.7846	-0.1272	-0.25
F10	C1-50	1.6622	0.2235	0.37
F11	C2+50	-0.4547	0.1314	-0.37
F12	C2-50	0.3748	-0.2132	0.538

Table 1: Time response specifications of single faults for test circuit

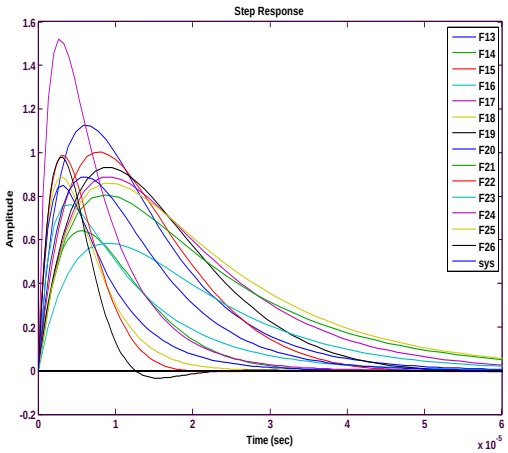

Fig. 5 Step response for multiple faults

Table 2: Time response specifications of single faults for test circuit

Fault ID	Fault components	Settling time *10^-5 sec	Peak	Delay time *10^-6 sec
F13	R2R5+50%	-0.5022	-0.2362	-0.05
F14	R2R5-50%	1.1081	0.2464	0.07
F15	R5C2+50%	0.2132	-0.1139	-0.45
F16	R5C2-50%	-0.1861	0.1261	0.539
F17	C1C2+50%	-2.1623	0	-0.72
F18	C1C2-50%	2.1624	0	0.71
F19	R1R3+50%	-0.3465	-0.0432	-0.76
F20	R1R3-50%	1.4227	0.0397	0.734
F21	R1R2C1+50	-3.5881	0.0809	-0.55
F22	R1R2C1-50	2.6684	-0.0986	0.649
F23	R1R2C2+50	-2.328	0.302	-0.7
F24	R1R2C2-50	1.3968	-0.6311	0.797
F25	R2C1C2+50	-3.6042	0.028	-0.69
F26	R2C1C2-50	2.4132	-0.0908	0.664
F27	Fault free	4.3247	0.888	1.42

VIII. CONCLUSION

An electronic circuit diagnostic system using artificial neural networks developed with circuit simulators has been proposed in this paper. The system shows the promise of using this approach for low cost test system development. Our study indicates that the proposed technique has a significant impact on analog fault diagnosis due to the selection of an optimal number of relevant features. This leads to neural network architectures with minimal size that can be trained efficiently and carry out fault diagnosis with a high degree of accuracy. By performing the time response test of the CUT under faulty and non faulty conditions, time response specifications for every category of faults is selected. Using suitable decision making preprocessor, the corresponding faulty signature is fed into the ANN which does the fault classification. The result of the proposed method applied to the Sallen key band pass filter circuit is quite encouraging. It would be very interesting to further enhance the method by considering the multiple faults case which are coming under ambiguity groups.

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